CLAIMS

1. A method of fabricating a memory device on a laminated circuit board wherein the laminated circuit board has a length, a width and a thickness, the method comprising:

laminating a metal layer to an insulating layer;

removing metal from the metal layer to define conductive paths, bonding pads, and rails, said rails defined along at least a portion of the edges of the length of the circuit board where no metal has been removed, said rails electrically isolated from said conductive paths and bonding pads; and,

etching the rails to remove metal therefrom.

2. The method of claim 1, wherein etching the rails includes removing all metal from the rails.

3. A method of fabricating a memory device on a laminated circuit board, wherein the laminated circuit board has a length, a width and a thickness comprising:

laminating a first metal layer to a first side of an insulating layer;

laminating a second metal layer to a second side of an insulating layer;

etching conductive paths and bonding pads onto the first metal layer to define at least one first side die site and at least one first side rail wherein said first side rail comprises a continuous strip of said first metal layer that is electrically isolated from said at least one first side die site;

etching conductive paths and bonding pads onto the second metal layer to define at least one second side die site and at least one second side rail, wherein said

second side rail comprises a continuous strip of said second metal layer that is electrically isolated from said at least one second side die site; and,

etching either said at least one first side rail, said at least one second side rail, or both said at least one first side rail and said at least one second side rail to remove at least a portion of the metal.

4. The method of claim 3, wherein etching conductive paths and bonding pads onto the first metal layer for at least one first side die site comprises removing metal from the first metal layer, resulting in forming rails along edges of the length of the first metal layer where the rails have no metal removed and wherein etching conductive paths and bonding pads onto the second metal layer for at least one second side die site comprises removing metal from the metal layer, resulting in forming rails along edges of the length of the second metal layer where the rails have no metal removed.

5. The method of claim 3, wherein etching the rails comprises removing sections of metal from the rails.

6. The method of claim 3, wherein etching the rails comprises removing all metal from the rails.

7. A method of forming a circuit board comprising:

forming a circuit board having an insulating layer sandwiched between a first conductive layer and a second conductive layer;

etching said first conductive layer defining a first site comprising a first patterned area of conductive traces, and a first generally rectangular rail extending adjacent to a first edge of said first conductive layer spanning substantially the length thereof, said

first rail electrically isolated from said first patterned area and comprises gaps etched into said first conductive layer; and,

etching said second conductive layer defining a second site comprising a second patterned area of conductive traces, a third generally rectangular rail extending adjacent to a first edge of said second conductive layer spanning substantially the length thereof, and a fourth generally rectangular rail extending adjacent to a second edge of said second conductive layer spanning substantially the length thereof, said third and fourth rails electrically isolated from said second patterned area and comprise gaps etched into said second conductive layer.

8. A method of forming a circuit board according to claim 7, further comprising:

a second generally rectangular rail extending adjacent to a second edge of said first conductive layer spanning substantially the length thereof, said second rail electrically isolated from said first patterned area and comprises gaps etched into said first conductive layer.

9. A method of fabricating a circuit board comprising:

forming a first layer of conductive material over an insulating layer;

removing portions of said conductive material of said first layer to define a first circuit pattern and a first rail area that is electrically isolated from said first circuit pattern; and,

removing portions of said conductive material of said first layer from said first rail area.

10. The method of claim 9, wherein said first rail area is positioned generally adjacent to a first edge of said circuit board, and spans at least a portion of the length of said first edge.

11. The method of claim 9, further comprising:

removing portions of said conductive material of said first layer to define a second rail area that is electrically isolated from said first circuit pattern and said first rail area; and,

removing portions of said conductive material of said first layer from said second rail area.

12. The method of claim 11, wherein said second rail area is positioned generally adjacent to a second edge of said circuit board, and spans at least a portion of the length of said second edge.

13. The method of claim 11, further comprising:

forming second layer of conductive material over said insulating layer opposite said first layer;

removing portions of said conductive material of said second layer to define a second circuit pattern and a third rail area that is electrically isolated from said second circuit pattern; and,

removing portions of said conductive material of said second layer from said third rail area.

14. The method of claim 13, further comprising:

removing portions of said conductive material of said second layer to define a fourth rail area that is electrically isolated from said second circuit pattern and said third rail area; and,

removing portions of said conductive material of said second layer from said fourth rail area.

15. The method of claim 9, further comprising:

forming second layer of conductive material over said insulating layer opposite said first layer;

removing portions of said conductive material of said second layer to define a second circuit pattern and a second rail area that is electrically isolated from said second circuit pattern; and,

removing portions of said conductive material of said second layer from said second rail area.